AMENDMENTS TO THE CLAIMS

Claims 1-10 (canceled)

Claim 11. (currently amended): A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a first sample-and-hold circuit for sampling and storing signals from pixels in a first column;

a second sample-and-hold circuit for sampling and storing signals from pixels in a second column;

an operational amplifier-based charge sensing circuit, associated only with the first and second columns in the array, that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter, associated only with the first and second columns in the array, for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converter including a comparator and a first binary-scaled capacitor network;

wherein

the capacitors in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is

coupled to a second input of the comparator, and

each of the capacitors in the first capacitor network has an associated latch circuit for storing a bit corresponding to a differential signal for a pixel sampled by the first sample-and-hold circuit while a differential signal for a pixel sampled by the second sample-and-hold circuit is amplified and converted to a corresponding digital signal.

Claims 12-13 (canceled)

Claim 14. (currently amended): A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a first sample-and-hold circuit for sampling and storing signals from pixels in a first column;

a second sample-and-hold circuit for sampling and storing signals from pixels in a second column;

an operational amplifier-based charge sensing circuit, associated only with the first and second columns in the array, that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit;

an analog-to-digital converter, associated only with the first and second columns in the array, for converting the differential output to a corresponding digital signal using a

successive approximation technique, said analog-to-digital converter including a comparator and a first binary-scaled capacitor network; and

a calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitors in the first network share a common node coupled to a first input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator, and

the calibration network selectively can be enabled to provide a DC shift to the common node to ensure that the signal for canceling the comparator offset appears as a positive voltage.

Claim 15. (cancel):

Claim 16. (currently amended): A circuit for reading out values of pixels from an active pixel sensor array, the circuit comprising:

a first sample-and-hold circuit for sampling and storing signals from pixels in a first

column;

a second sample-and-hold circuit for sampling and storing signals from pixels in a second column;

an operational amplifier-based charge sensing circuit, associated only with the first and second columns in the array, that selectively provides an amplified differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit;

an analog-to-digital converter, associated only with the first and second columns in the array, for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converter including a comparator and a first binary-scaled capacitor network; and

a calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitors in the first network share a common node coupled to a first input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator, and

one side of each capacitor in the first capacitor network selectively can be

connected to a first reference voltage, and wherein one side of each capacitor in the second capacitor network selectively can be connected to a second reference voltage different from the first reference voltage.

Claims 17-23 (canceled)

Claim 24. (currently amended): A CMOS imager comprising:

an array of active pixel sensors, wherein each pixel is associated with a respective column in the array; and

a plurality of readout circuits for reading out values of pixels from the active sensor array, wherein each readout circuit is associated with a respective pair of first and second columns in the array, and wherein each circuit includes:

a first sample-and-hold circuit for ~~fro~~ sampling and storing signals from pixels in the first column;

a second sample-and-hold circuit for ~~fro~~ sampling and storing signals from pixels in the second column;

an operational amplifier-based charge sensing circuit that selectively provides an amplified ~~amplifier~~ differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter for converting the differential output to a corresponding digital signal using a successive approximation technique, said

analog-to-digital converting including a comparator and a first binary-scaled capacitor network,

wherein

the capacitor in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator, and

each of the capacitors in the first capacitor network has an associated latch circuit for storing a bit corresponding to a differential signal for a pixel sampled by the first sample-and-hold circuit while a differential signal for a pixel sampled by the second sample-and-hold circuit is amplified and converted to a corresponding digital signal.

Claims 25-27 (canceled)

Claim 28. (currently amended): A CMOS imager comprising:

an array of active pixel sensors, wherein each pixel is associated with a respective column in the array; and

a plurality of readout circuits for reading out values of pixels from the active sensor array, wherein each readout circuit is associated with a respective pair of first and second columns in the array, and wherein each readout circuit includes:

a first sample-and-hold circuit for ~~fro~~ sampling and storing signals from pixels in the first column;

a second sample-and-hold circuit for ~~fro~~ sampling and storing signals from pixels in the second column;

an operational amplifier-based charge sensing circuit that selectively provides an amplified ~~amplifier~~ differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converting including a comparator and a first binary-scaled capacitor network,

a calibration network for providing a signal to cancel an offset of the comparator, said calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitor in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network, and

the calibration network selectively can be enabled to provide a voltage shift to the common node to ensure that the signal for ~~fro~~ canceling the comparator offset appears as a positive voltage.

Claim 29. (currently amended): A CMOS imager comprising:

an array of active pixel sensors, wherein each pixel is associated with a respective column in the array; and

a plurality of readout circuits for reading out values of pixels from the active sensor array, wherein each readout circuit is associated with a respective pair of first and second columns in the array, and wherein each readout circuit includes:

a first sample-and-hold circuit for ~~fro~~ sampling and storing signals from pixels in the first column;

a second sample-and-hold circuit for ~~fro~~ sampling and storing signals from pixels in the second column;

an operational amplifier-based charge sensing circuit that selectively provides an amplified ~~amplifier~~ differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converting including a comparator and a first binary-scaled capacitor network,

a calibration network for providing a signal to cancel an offset of the comparator, said calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitor in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network, and

one side of each capacitor in the first capacitor network selectively can be connected to a first reference voltage, and wherein one side of each capacitor in the second capacitor network selectively can be connected to a second reference voltage different from the first reference voltage.

Claim 30. (currently amended): A CMOS imager comprising:

an array of active pixel sensors, wherein each pixel is associated with a respective column in the array; and

a plurality of readout circuits for reading out values of pixels from the active sensor array, wherein each readout circuit is associated with a respective pair of first and second columns in the array, and wherein each readout circuit includes:

a first sample-and-hold circuit for ~~fro~~ sampling and storing signals from pixels in the first column;

a second sample-and-hold circuit for ~~fro~~ sampling and storing signals from pixels in the second column;

an operational amplifier-based charge sensing circuit that selectively provides an amplified ~~amplifier~~ differential output signal based on signals sampled either by the first sample-and-hold circuit or the second sample-and-hold circuit; and

an analog-to-digital converter for converting the differential output to a corresponding digital signal using a successive approximation technique, said analog-to-digital converting including a comparator and a first binary-scaled capacitor network,

a calibration network for providing a signal to cancel an offset of the comparator, said calibration network including a second binary-scaled capacitor network used to successively approximate and store the offset of the comparator,

wherein

the capacitor in the first network share a common node coupled to a first input of the comparator,

the amplified differential output signal from the charge sensing circuit is coupled to a second input of the comparator,

the capacitors in the second capacitor network share a node in common with the capacitors in the first capacitor network, and

the calibration network selectively can be enabled to provide a post-gain offset for the differential output signal from the charge sensing circuit.

Claims 31-37 (canceled)